IN THE CLAIMS:

Claim 1 has been amended herein. All of the pending claims 1 and 2 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1. (Currently amended) A method for improved differential electrical noise reduction for an integrated circuit device having a memory having multiple vertical levels of circuitry, the memory having at least four arrays of memory cells, each array of memory cells being substantially equally spaced from an adjacent array of memory cells, each array of memory cells including a plurality of memory cells and at least four pairs of digitlines, each pair of digitlines including a first digitline and a second digitline, the first digitline and the second digitline being substantially vertically aligned in an upper conductive level and a lower conductive level of the integrated circuit device, the first digitline and the second digitline of each pair of digitlines each connected to an equal number of the plurality of memory cells in each array of memory cells, the method comprising:

electrically balancing the first digitline and the second digitline of each digitline pair of the at least four pairs of digitlines to balance the electrical noise therebetween by vertically twisting the first digitline and the second digitline of each pair of digitlines of the at least four pairs of digitlines between arrays of the at least four arrays of memory cells in a twist region located between each array of the at least four arrays of memory cells, a first pair of digitlines and a third pair of digitlines of the at least four pairs of digitlines vertically twisted in the twist region located between a first array of memory cells and a second array of memory cells and vertically twisted in the twist region located between a third array of memory cells and a fourth array of memory cells while a second pair of digitlines and a fourth pair of digitlines of the at least four pairs of digitlines are vertically twisted in the twist region located between the second array of memory cells and the third array

of memory cells, the electrically balancing including connecting an equal number of memory cells to a portion of one of the first digitline and the second digitline of a pair of digitlines of the at least four pairs of digitlines when located ~~in a~~ in the lower conductive level of an array of the at least four arrays of memory cells.

2. (Previously presented) The method of claim 1, further comprising:

isolating adjacent memory cells of an array of the at least four arrays of memory cells using an isolation region comprising a plurality of isolation transistors, each isolation transistor having a gate biased to a predetermined voltage.

IN THE DRAWINGS:

The attached sheets of drawings include changes to FIGS. 17 and 18. These sheets replace the original sheets including FIGS. 17 and 18.

Specifically, FIG. 17 has been revised to change the reference numeral "14" (appearing in the top central portion) to --16-- and to change the reference numeral "16" (appearing in the right-hand portion) to --14--; and FIG. 18 has been revised to change the reference numeral "14" (appearing in the central portion) to --16--, to change the reference numeral "16" (appearing in the right-hand portion) to --14--, to delete the word "fieldpoly" (appearing in the bottom left-hand portion), and to insert the words --field poly-- and a corresponding lead line arrow indicating the structure appearing directly above the "field oxide" structure in the left-hand portion of the figure. No new matter has been added.